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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,508	09/19/2003	Nazar Syed Haider	110348-133032	9177

25943 7590 11/18/2004

SCHWABE, WILLIAMSON & WYATT, P.C.  
PACWEST CENTER, SUITES 1600-1900  
1211 SW FIFTH AVENUE  
PORTLAND, OR 97204

EXAMINER

ENGLUND, TERRY LEE

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/666,508

Applicant(s)

HAIDER ET AL.

Examiner

Terry L Englund

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 19 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10, 15-20 and 23-27 is/are rejected.
- 7) ☒ Claim(s) 11-14, 21 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11032003.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Objections*

Claims 3-7, 10-14, and 20-24 are objected to because of the following informalities: To improve word flow, it is suggested “a first, a second, and a third...device” on each of lines 2 and 3 of claim 3 be changed to --first, second, and third...devices--. For consistent labeling throughout the claims, it is suggested “reference voltage” on line 1 of claim 4 be changed to --voltage reference--. Since the generator and originator circuits of claim 1 already comprise (or include) elements (i.e. the generator comprises the first/second originator circuits as well as the selector circuit; and each originator circuit includes a plurality of channel devices), it is suggested the term --further-- be added after the second occurrence of “generator” in claim 4 (line 1); “circuit” in claim 4 (line 3); and “circuit” in claim 5 (line 1). Also for consistent labeling, “source voltage” on line 5 of claim 4 should be changed to --supply voltage-- to correspond to “supply voltage” recited on line 2 of the same claim. To improve word flow, it is suggested the term --to-- be added after “coupled” on line 7 of claim 5. Claim 7, line 1 “reference voltage generator” should be changed to --voltage reference generator further-- for consistent labeling, and since the generator of claim 1 already comprises (or includes) other elements (e.g. see the reasoning applied to claims 4-5 above). Similar to claim 3, it is suggested each occurrence of “a first, a second, and a third...device” on lines 1-3 of each of claims 10 and 20 be changed to --first, second, and third...devices--. For consistent labeling throughout the claims, it is suggested “reference voltage generator” on line 1 of claim 11 be changed to --reference generator further-- to correspond to the “reference generator” within claim 8 (lines 4 and 7) that already includes the originator circuits/channel devices. Similarly, --further-- should be added

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after the second occurrence of "circuit" on line 1 of claim 12 since the circuit already includes channel devices (e.g. see claim 8, lines 14-15), and --to-- should be added after "coupled" on line 7 of claim 12 to improve word flow. Claim 14, line 1 "reference voltage generator" should be --reference generator further-- for the same type of reasoning as applied to claim 12, line 1.

Similar to claims 11, 12, and 14, the following changes to claims 21, 22, and 24 are suggested:

1) change "reference voltage generator" to --reference generator further-- on line 1 of both claims 21 and 24; add --further-- after "circuit" on line 1 of claim 22, and add --to-- after "coupled" on line 7 of the same claim. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The use of "based upon an output signal to the hysteresis circuit" in claim 1, lines 5-6 is confusing for several reasons: 1) It is believed the originator circuits and selector circuit are part of the hysteresis circuit. Without them, there is no hysteresis circuit. Therefore, does this limitation imply that the hysteresis circuit and the voltage reference generator are two distinct circuits? 2) Where does this "output signal" come from? For example, is it an output signal (from an unidentified circuit) that is applied to the hysteresis circuit as an input signal of the hysteresis circuit, or is it an output signal from the hysteresis circuit? Although it is understood a plurality of channel devices can have a minimum of two (i.e.

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first and second/last) devices, the use of “the third p-channel device” in claim 4, line 6 implies the plurality must include at least three devices. However, how can there be a third transistor if the first plurality of claim 2 might only comprise two devices? In this case, was claim 4 meant to depend on claim 3, which clearly identifies first-third devices? [Note: Claims 11 and 21, which correspond to claim 4, depend on claims 10 and 20, respectively, wherein claims 10 and 20 each clearly recite the first-third devices, thus they correspond to claim 3.] Similar to claim 4 described above, the use of “the third n-channel device” on line 5 of claim 5 implies the second plurality includes a minimum of three devices. [Note: If the dependency of claim 4 is changed to claim 3, this problem in claim 5 will be overcome.]

Claim 23 recites the limitation “the first and second reference voltage nodes” in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. Was this claim meant to depend on claim 22 that recites “a second reference voltage node” on lines 1-2?

Claim 24 recites the limitations “the first reference voltage node” and “the second reference voltage node” on lines 5 and 6-7, respectively with insufficient antecedent basis for these limitations in the claim. Was this claim also meant to depend on claim 22?

Dependent claims carry over any 112 type rejection(s) from any claim(s) upon which they depend.

### ***Claim Rejections - 35 USC § 103***

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

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the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 8-10, 15-20, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al. (Chao), in view of Kaneko et al. (Kaneko). Fig. 3 of Chao shows a hysteresis circuit 12 comprising a sensing amplifier 30 for generating output signal OUT at output 36, and a (voltage) reference generator 32 coupled to output 36 for generating an output reference voltage on line 35. Sensing amplifier 30 has input N1 coupled to receive input signal IN, and input N2 coupled to receive the output reference voltage on line 35. Fig. 5 shows more details of (voltage) reference generator 32, which comprises a selector (not labeled but understood to be "51" from the descriptions on column 5, lines 38 and 44-51) that provides one of two reference voltages REFH, REFL as the output reference voltage on line 35 based on output signal OUT. Fig. 6 shows details of sensing amplifier 30 and (voltage) reference generator 32. Although the reference does not clearly show or disclose first/second originator circuits for generating the first/second reference voltages VREFH/VREFL, respectively, Chao discloses "those skilled in the art can design several suitable implementation of voltage reference generator 52 without undue experimentation" (i.e. see column 5, lines 41-44); and VREFH/VREFL are preselected (e.g. see column 6, lines 58-62; and column 7, lines 1-10; and the REF

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waveform shown in Fig. 7). Kaneko shows reference voltage generating circuits in Figs. 6C-6D which provide a respective reference voltage output  $\emptyset 2$  (e.g. see column 6, line 4). Therefore, it would have been obvious to one of ordinary skill in the art that reference voltages VREFH/VREFL of Chao's Fig. 6 circuit could be provided by corresponding first/second originator circuits of Kaneko (Figs. 6C/6D). First originator circuit (Fig. 6C) comprises first-third p-channel devices PM22, PM21-1, and PM21-n; and second originator circuit Fig. 6D comprises first-third n-channel devices NM22, NM21-1, and NM21-n. Therefore, the modified circuit would comprise a first originator circuit (Kaneko's Fig. 6C) for generating first reference voltage VREFH; a second originator circuit (Kaneko's Fig. 6D) for generating second reference voltage VREFL; and a selector circuit (52 of Chao's Fig. 6, or the unlabeled multiplexer 51 in Chao's Fig. 5). From Figs. 3-6 of Chao's reference, and their related descriptions (e.g. see column 4, lines 45-56, and column 5, lines 16-29), one of ordinary skill in the art would understand the selector circuit provides either the first or second reference voltage (VREFH or VREFL) based on output signal OUT transitioning (e.g. falling (i.e. making a high-to-low transition); and rising (i.e. making a low-to-high transition)). Therefore, claims 1-3, and 8-10 are rendered obvious. [Note: Chao's Fig. 3 circuit corresponds to block 50 shown in the applicants' own Fig. 7.] The circuits of Kaneko's Figs. 6C-6D could be used to provide reference voltages VREFH/VREFL to ensure the p-/n-channel devices of Figs. 6C/6D would closely correspond (e.g. have similar operating characteristics with respect to temperature and fabrication) to p-/n-channel devices 65P/65N of Chao's selector type circuit shown in Fig. 6. The values of VREFH and VREFL would depend on what hysteresis levels were desired (e.g. see column 5, lines 60-63 of Chao). Fig. 2 of Chao shows hysteresis circuit 12 (e.g. of Fig. 3) as part of bus interface unit 28 in

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processor 11 (also shown in the computer system of Fig. 1). Also, column 1, lines 6-15 relates the invention to integrated circuits. Therefore, it would be obvious to one of ordinary skill in the art that the hysteresis circuit is in an integrated circuit, and that integrated circuit can be considered a microprocessor, thus rendering claims 15-16 obvious. Fig. 2 shows integrated circuit 11 having input circuit 12 (which corresponds to the Chao/Kaneko circuit circuitry with respect to the reference generator/hysteresis circuit/first-second originator circuits/first-second reference voltages/first-second pluralities of channel devices as previously described); main memory 14 (disclosed by Chao as including one or more DRAMs – i.e. see column 2, lines 56-59) coupled to integrated circuit 11 via bus 15; and input/output interface 28 also coupled to integrated circuit 11. Therefore, claims 17-20 are rendered obvious. Note: The input/output module can be related to devices 17/18 shown in Fig. 1 being coupled to central processing unit 11 and main memory 14 via bus 15. Deeming Chao's 54 and 55 as the first/second reference voltage nodes, selector circuit 51 (not labeled in Chao's Fig. 5) or 52 (of Chao's Fig. 6) is coupled between those nodes, thus rendering claim 23 obvious. From Fig. 6, one of ordinary skill in the art would realize selector circuit 52 of the reference generator includes output reference voltage node 35; fourth p-channel device 65P with its drain coupled to node 35 and its source coupled to first reference voltage node 54; and fourth n-channel device 65N with its drain coupled to node 35 and its source coupled to second reference voltage node 55, rendering claim 24 obvious. Chao's processor 11 can be deemed a microprocessor (e.g. see related column 1, lines 66-67; and column 3, lines 53-55), and input/output interface 28 can be considered as comprising a networking interface. Therefore, respective claims 25 and 26 are rendered obvious. It would have been obvious to one of ordinary skill in the art that the Chao/Kaneko system could



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be used in a selected one of a set-top box, entertainment unit, and DVD player, thus rendering claim 27 obvious. These are considered intended use, wherein the system can be used to provide reliable control (e.g. fast operation; minimal noise; and less sensitivity to process, temperature, and voltage variations – e.g. see column 1, lines 22-29; column 2, lines 31-35; column 6, lines 16-27; and column 8, lines 42-43) to whatever application it is employed in.

No claim is allowable as presently written.

***Allowable Subject Matter***

However, claims 11-14, and 21-22 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Also, their respective objections described above should be addressed/corrected. There is presently no motivation to modify or combine any prior art reference(s) to have the specific structure with respect to the first-third channel devices as recited within each of claims 11, and 21 (upon which claims 12-14, and 22, depend respectively).

Also, claims 4-7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to have the specific structure of the first-third channel devices as recited within claim 4 (upon which claims 5-7 depend).

**Prior Art**

The other prior art references on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although not used in any formal rejections described

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above, p-/n-channel devices of Holzer et al.'s Figs. 13/5 could have been used as originator circuits generating first/second reference voltages to be applied to a selector circuit (e.g. Cao's Fig. 6 p-/n-channel selector 65P/65N). Also, Ueda's Fig. 16 circuit (with four n-channel devices) and Fig. 24 (with four p-channel devices) could have been used to provide their respective reference voltage to the selector circuit. Therefore, since both of these references clearly show/disclose circuits that could be used as originator circuits for providing their respective reference voltage to a selector circuit, these references should be carefully reviewed and considered.

The prior art references cited on the IDS submitted on Nov 3, 2003 were carefully reviewed and considered. Although the references of Bazes and Taub et al. disclose the selection of a reference voltage between upper and lower limits, neither reference clearly shows or discloses anything specific about hysteresis, or that the selection is actually between two distinct reference voltages. Although not used in any formal rejection described above, the Falconer reference clearly shows a hysteresis type circuit in Fig. 6 with a selection circuit 610 for selecting between first/second reference voltages  $V_{high}/V_{low}$ . However, the reference does not specifically cite "hysteresis", and although Figs. 4b/4c show first/second originator circuits each having first-third channel devices, each circuit has the same type channel devices (e.g. n-channel are shown). Column 7, lines 20-23 indicate that p-channel devices can also be used, but the disclosure does not clearly indicate that p-channel devices can be used for one originator circuit, while n-channel devices can be used for the other originator circuit. However, depending on what type of levels would be desired for the reference voltages, one of ordinary skill in the art could find it obvious to use one channel type circuit to provide one of the references voltages,

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and use another channel type circuit to provide the other reference voltage. Therefore, the Falconer reference should be reviewed and reconsidered with respect to the possibility that the two reference voltages applied to the Fig. 6 circuit could be provided by originator circuits having different channel devices.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

9 November 2004



TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800